# Clock divider module

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| Input name | Full name | Purpose |
| old\_clock | Old clock | This is parent clock that the new clock is to be generated from. |
| reset | Reset | Reset the counters to 0 when the line drops to 0 |

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| Parameter name | Full name | Purpose |
| clock\_div | Clock frequency division factor | This is the number that the clock frequency is to be divided down by to achieve the new clock frequency. |

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| Output name | Full name | Purpose |
| new\_clock | New clock | This is the new slower clock that is generated by the counter. |

## General Overview.

This module works by incrementing a counter on every rising edge of the old clock. When the counter reaches the limit set by the clock\_div parameter it resets. A 50:50 duty cycle is achieved by setting the output high when then counter is below half of the clock\_div.

## Detailed descriptions.

* The register size is set to be 32 bit so that the fastest clock on the board the 50 MHz can be divided down to speeds greatly below 1 Hz while setting it to be only 16 bit resulted in limitations to the maximum division. Ultimately as the parameter is a set value the register will be down sized during optimization.
* The clock\_div parameter has 1 subtracted from it when used in the reset and output as in digital logic you count from 0. (I.e. 0 to 59 for 60) by subtracting 1 we correct for this.